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PART 4

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The first 3 sections have covered the General Concept, the Power Supply and the Sync Pulse Board.

This section deals with the Address Counters and Registers in theory and practice.

As explained in Part 1 we have to produce discrete sets of binary codes which designate portions of the television display raster to the different character cells. These are called the Character "Column" and "Row" Addresses respectively. We have also to produce similar codes which designate portions within each character cell. You will remember that each cell comprises a matrix of 6 picture points in width by 8 picture points in height. Each of the six vertical picture point columns needs a code to tell the multiplexer the sequence in which they must appear when they are assembled into the final video signal. The Read Only Memory also needs to know which row of picture points (within the cell) it should be operating on hence eight binary codes are required to identify them.

These address codes have to be produced in a very regular fashion and in exact synchronism with the television raster so that they always relate to precise positions on the screen in the final display.

Fig. 14 is a schematic of the address code generators, which we call counters. The word counter is a perfect description because that is all they are. Within the circuit there are four fairly straightforward binary divider chains. They vary from ordinary divider chains in that some of them do not start at a count of zero and all of them are forced to reset before they have completed their natural counting cycle.

MULTIPLEXERS

Take the Multiplexer Address Counter for instance. This is IC20, a four stage binary divider IC. The first stage is not used because we need to divide the 4MHz clock by 6 to define the codes for each of the six picture points within the width of the cell. To count on a scale of six only, a 3 stage counter is required which has a maximum range of eight. To get it to cycle on six we have to force it into a reset condition after the count of "5". This is done by IC21b in conjunction with IC21a.

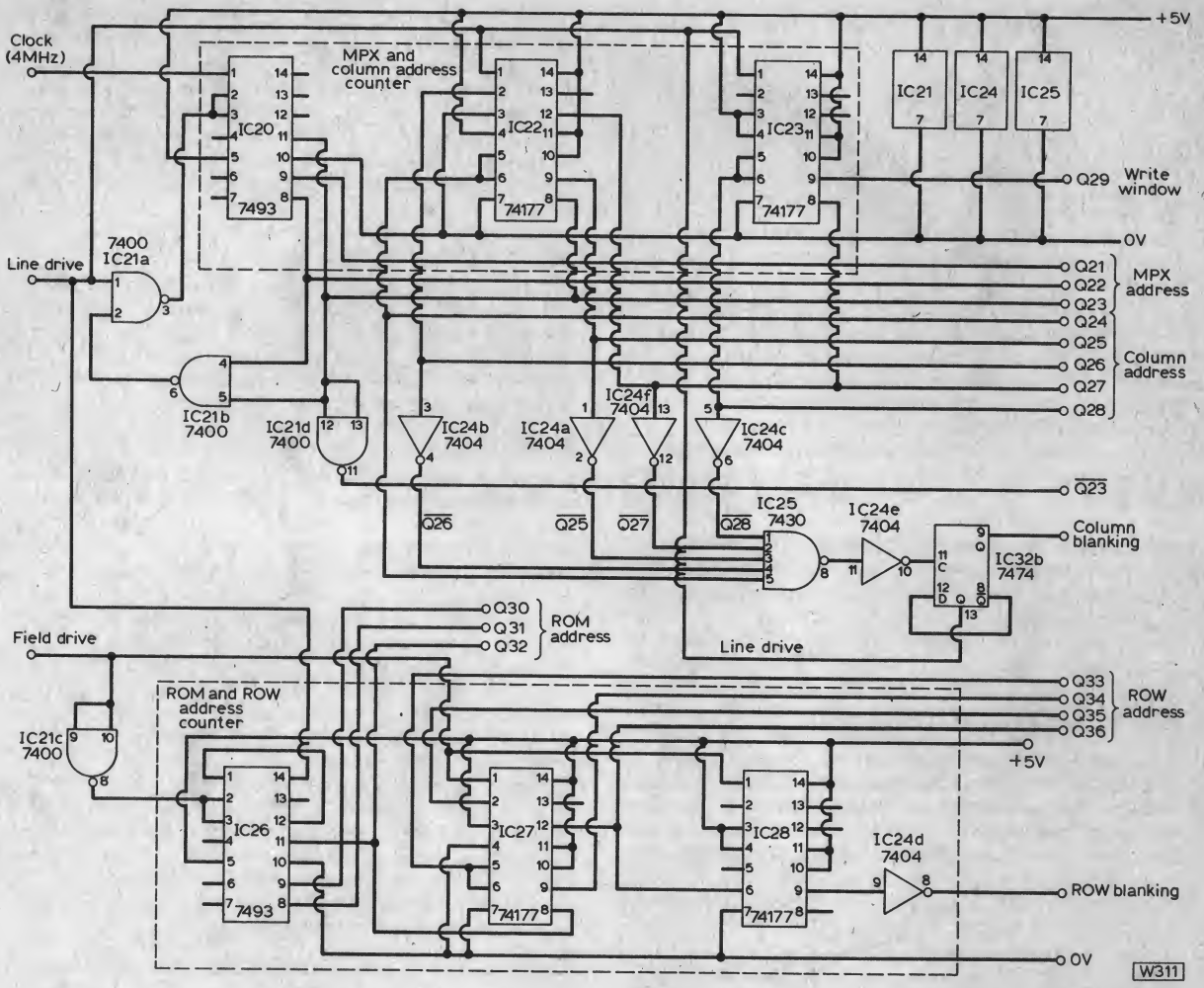
To ensure that the counter always starts at a count of zero at the beginning of a television raster line (this is to ensure synchronism) we use the line sync pulse (Line Drive) to override the internally generated reset. This is particularly important because there are a potential 256 picture points along a line (including the line sync period) and this number is not exactly divisable by six. Without an overriding reset at the start of each line the counter would precess relative to the lines of the display and the final result would be rubbish. IC21a accepts the line drive reset as well as the "scale of six" reset from IC21b and feeds a reset signal to IC20.

If you refer to Fig 15, you will see the waveforms that are generated by the three outputs of IC20. We call these the Multiplexer Address lines and they are designated Q21, Q22 and Q23. Notice that, apart from the reset to zero period when line drive is active, Q21 is simply a divide by two of the 4MHz clock. Q22 does not get a chance to take up its second "high" before the counter is reset on the scale of six and the "high" of Q23 is curtailed by the reset. This sequence requires 6 clock pulses after the line drive signal has ended and if the three address lines are looked at as binary numbers you can see the six discrete codes that they represent in the table under the region marked as the first "Cell Width". The code 000 describes the most left-hand picture along a row in the cell while 001 represents the second from the left and 101 represents the sixth. The counter is then reset to 000 and this describes the most left-hand picture point of the next cell and so on.

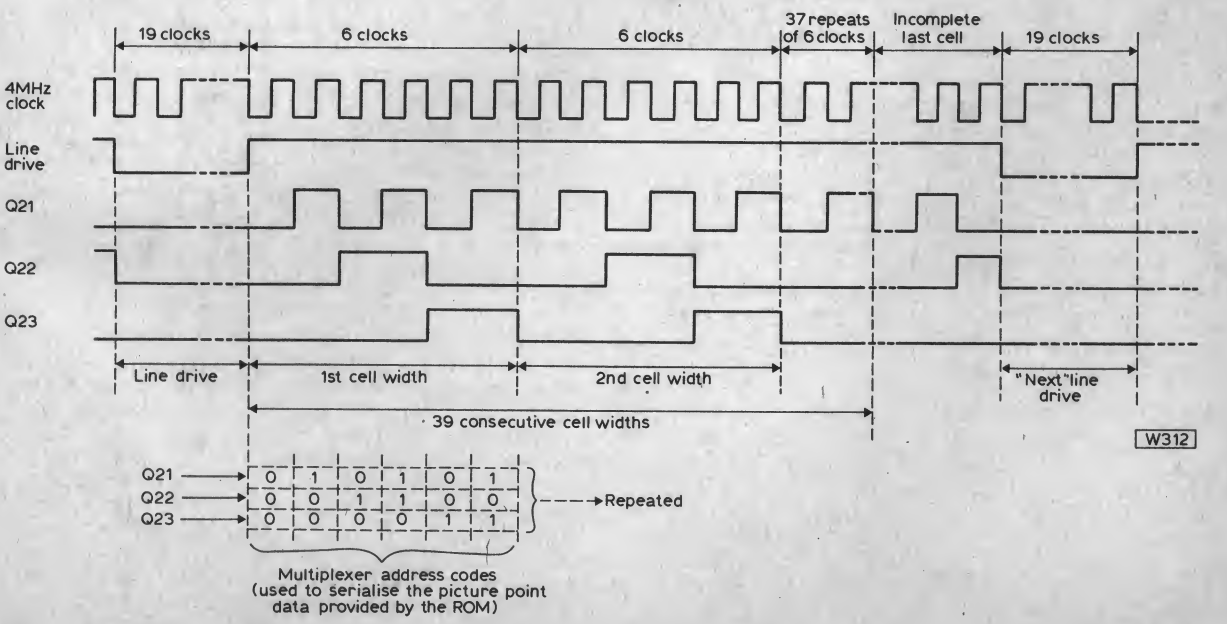
COLUMN ADDRESS

A total of 39 complete cells can be described along a television raster line in this manner but, as mentioned before, there is an incomplete cell on the extreme right hand end of the raster line which only has three picture points. The line drive reset takes over in the middle of this cell and resets the counter in readiness for the next television line.

The first five cells along a raster line are not used for display as they form the left hand margin while the last two complete cells plus the forshortened cell form the right hand margin. The fact that the last



▲ *Fig. 14. Schematic diagram of the Address Counters.*



▼ *Fig. 15. The waveforms from IC20 (modulo 6 counter).*

cell along the line is shorter than the rest does not affect the appearance of any character as it falls in the margin.

The Q23 signal occurs once and once only in each cell and as it has a transition to zero at the end of every cell it can be used as the signal source for counting the cells across the width of the screen. This counting is carried out by IC22 and IC23 which are used as a five stage binary divider to generate the address codes for each column of cells. It is convenient to use the code 00000 to describe the first cell which will contain a character of the final display.

As said before the first five cells after the line drive signal are to form the margin therefore we need the code 0000 to occur on the SIXTH cell. To achieve this we ensure that the five stages of the counter are reset to a predetermined code on receipt of the line drive signal.

The way this counter operates can be seen in the waveforms of Fig. 16. The top two signals (Line Drive and Q23) are the same as those shown in the previous figure but this time we have put in all the Q23 signals for a single television line. Remember that it occurs only once in each cell therefore every time it reverts to zero in this diagram it corresponds to the right hand edge of a character cell. These transitions are counted by the first five stages of the Column Address Counter in binary form; the outputs of the counter being Q24, 25, 26, 27 and 28 respectively. Line Drive is used to reset the counter so that all stages except Q26 are at "1".

This means that at the end of the fifth cycle of Q23 the output code of the counter, taken as a whole, will be 00000, the zero address position for the first display character cell. Note that this is how the five character cell wide left hand margin is formed. The counter then proceeds in conventional binary fashion for a further 32 cycles of Q23 defining the 32 different column address codes for the character cells across the width of the screen. These codes are shown in the table at the foot of the diagram.

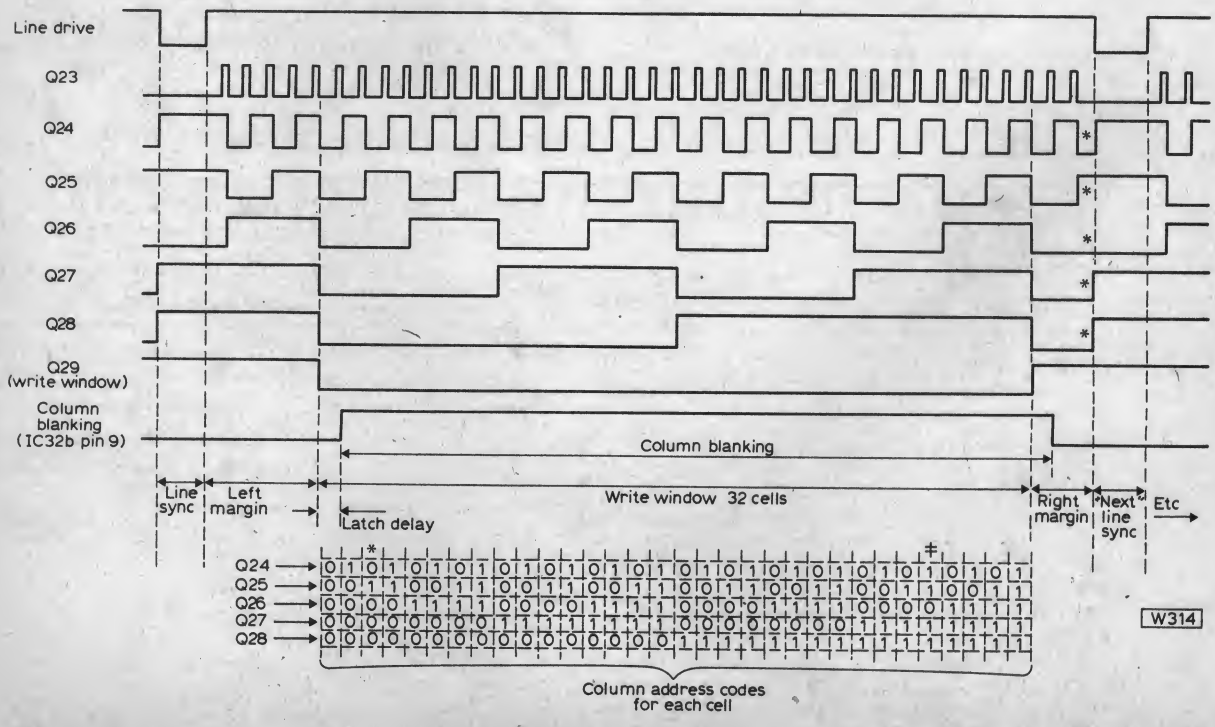
After the latter 32 cycles of Q23 we receive two more before the next line drive pulse comes along to reset the counter to its start position. These two extra pulses conveniently form the right hand margin.

WRITE WINDOW

Apart from the address codes for the columns of character cells we also obtain a special signal from the next stage of this counter (Q29) this we call "Write Window". The purpose of this signal is to prevent an ambiguous case occurring during the Write operation of the instrument.

You will note that the code for the third display character position is 00010 and this occurs briefly for a second time just before the occurrence of the line drive reset signal. This in itself is no problem except the pulse which is used to instruct the Random Access Memory to accept input data (the Write instruction) happens to fall in the middle of a character cell. As the last cell along the TV line is foreshortened—see Fig. 15—this writing instruction spreads into the code produced by the Column Address Counter during the reset period. This code is 11011 and is identical to that for the twenty-eighth display character position. If we did not take steps to prevent it happening, whenever we write something into address position 00010 the same character would appear further down the row in the position corresponding to the Address 11011! The simplest way of preventing this problem is to inhibit the writing pulse at all times except during the time called the Write Window which is defined by the signal Q29. You will see this signal entering the comparator later in this description.

Fig. 16. Waveforms from the Column Address Counter. Note that the code 00010, marked by an asterisk, also occurs immediately before the line sync period (see text).



MARGIN BLANKING

During the read cycle of the instrument the address counter will be going through all its code combinations and unless something is done about it we would get true addresses thrown up at the times of the left and right hand margins. The effect of this would be to repeat some of the characters (that have equivalent addresses) in the margins. In reality it does not matter if this happens as long as we don't see them, so we arrange to blank the video signal as we are going through the margin address positions. This is slightly complicated by the fact that we have to embody a character cell delay between addressing the Random Access Memory and displaying the information. This was mentioned in Part 1. The column blanking signal must therefore be one character cell delayed relative to the addresses. This is clearly seen in the bottom waveform of Fig. 16. This delayed waveform is generated by the circuitry associated with IC32b.

ROM ADDRESS

Having defined the horizontal positions of the cells we now have to prescribe Addresses to them to designate their vertical positions and at the same time generate lower level address codes to denote which of the eight rows of picture points within the cell is active (this is needed for the Read Only Memory). It is the latter which we produce first and we call it the ROM Address. The counter which produces it is IC26. You should refer also to Fig. 17.

Because each row of picture points within a cell is made up of two raster lines the first thing we do is divide the line rate by two. This is done by the first stage of IC26. We have not given a designation to this half line frequency signal as it does not play any further part in the circuitry but, if you have an oscilloscope, it can be seen at pin 12 of IC26.

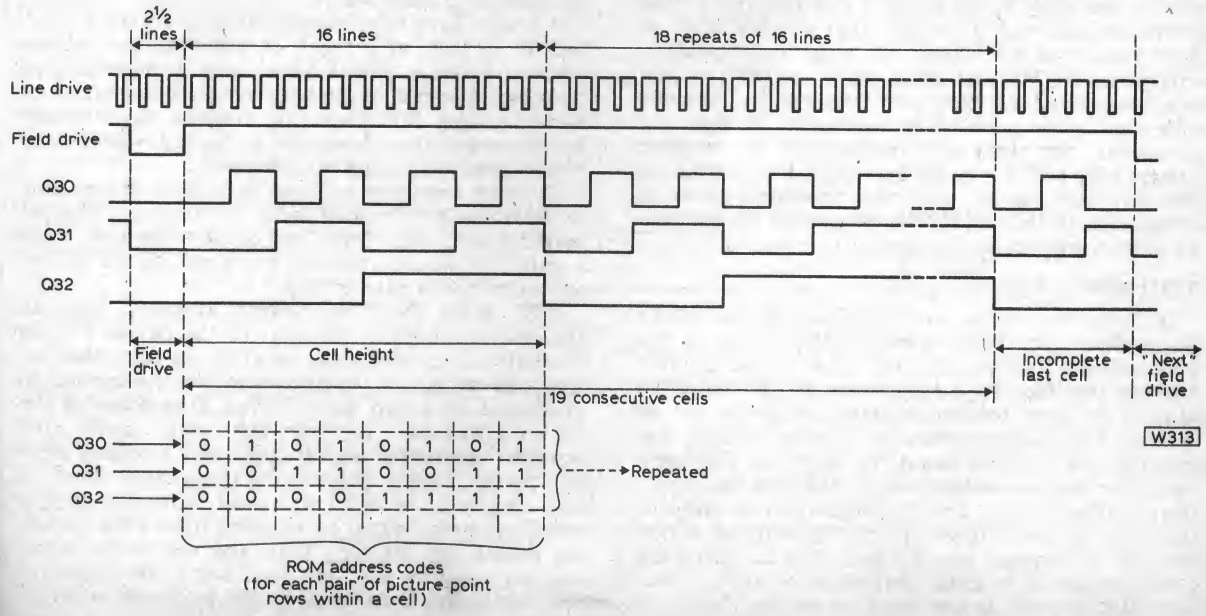
The following three stages of IC26 produce the ROM Address signals shown as Q30, Q31, and Q32 in Fig. 17. These three stages are reset to an "All Noughts" starting condition by the inverted field drive signal. This ensures synchronism with the field rate of the television raster. Conventional binary division takes place with the counter of IC26 completing 19 full cycles. It then starts an extra cycle but is unable to complete it before the next field drive signal, which resets the counter in readiness for the next field. There will be a short delay (half a line period) before the start of cycling for the next field—due to the staggering of line drive pulses brought about by our locked interlace system. On the third field this delay will not occur, but on the fourth it will be present again and so on.

ROW ADDRESS

One complete cycle of Q32 defines the height of a character cell and the eight codes generated by the Address lines are shown in the table of Fig. 17. As already mentioned we obtain "19 and a bit" cells; the top two and bottom "One and a bit" are reserved for top and bottom margins respectively so we require the Row Address for all the cells occurring on the THIRD row from top of the screen to be 0000.

An identical technique is used to that already described for the Column Address Counter. The four stages within IC27 give the Row Address as Q33, Q34, Q35 and Q36. Field drive is used to reset this counter to "All Ones" with the exception of Q33. Reference to Fig. 18 shows that this gives us an address of 0000 for the third row. The counter operates up to 16—producing the address for each row of cells—and then starts to re-cycle just before the next field drive pulse. For the same reasons as before we have to prevent the appearance of characters in the top and bottom margins so we use the first stage of IC28 to divide Q36 by two and this gives us (after inversion by IC24d) our Row Blanking signal. There is no need for this to be subjected to the delay that was needed in the case of the Column Blanking signal.

Fig. 17. The waveforms appearing at the outputs of IC26, the ROM Address Counter.



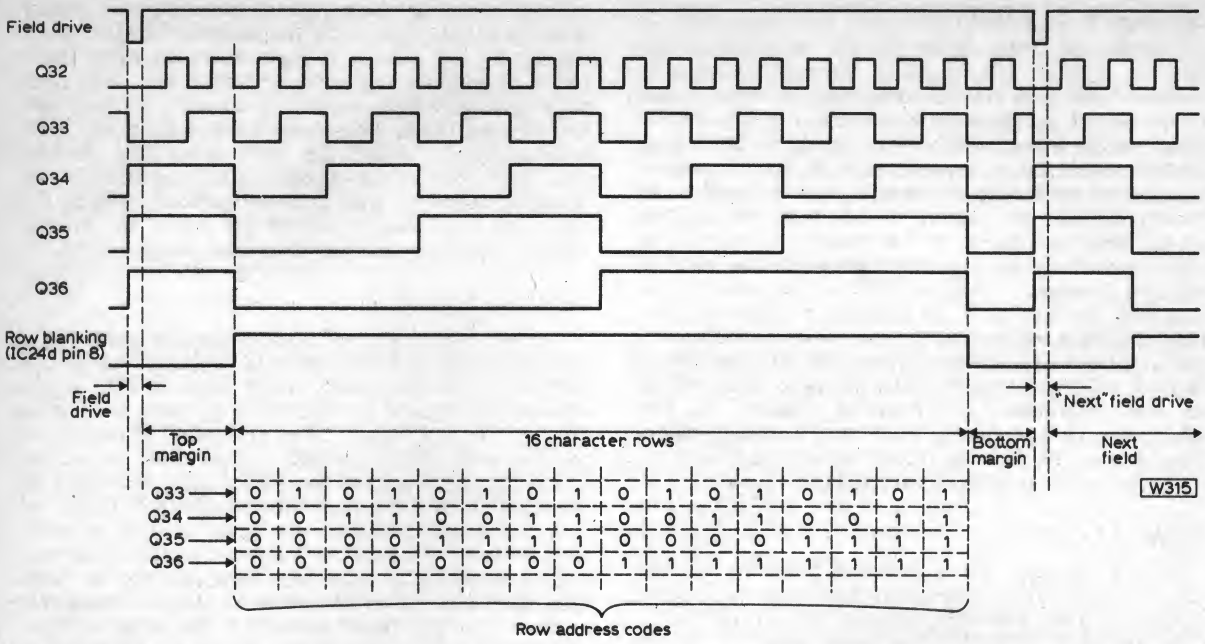


Fig. 18. The waveforms from the outputs of IC27 and IC28 (these form the Row Address Counter).

ADDRESS ROUTING

As might be expected the MPX Address codes are fed directly to the multiplexer (which will be described later), the ROM Address codes go straight to the Read Only Memory and the Column and Row Address codes go to the Random Access Memory to call up the correct data to describe the character that should be occurring at the prescribed place on the screen. The Column and Row Addresses are also fed to the comparator (Fig 19) to start the process of generating a writing signal.

CELL IDENTIFICATION

As explained in the first part of this series we have to keep a record of where on the screen we expect the next character to occur when we are typing into the system. Clearly every character cell can be described in terms of a Column and a Row Address code and a combination of any pair of these codes will be unique for a particular position on the screen. We can use a static register to hold any pre-determined code and compare its contents with the Column and Row Addresses as they are generated. Whenever the contents of the register exactly tally with the codes generated by the Address Counters we can say that the television raster is going through the cell that is designated by the code we have stored in the register.

ADDRESS REGISTERS

To keep life simple, and practical, we have split the register into two logical portions. One is the Row Address Register and the other is the Column Address Register. In a typewriter we do not often wish to go to a particular place on the screen at random but usually follow a certain pattern. For example we usually want to step to the next character position along a line (towards the right) after we have typed the last character. At the end of a line we want to return to the start of a new line (i.e. a carriage return) and then to step down a line. It should be clear that stepping along a line from left to right is the same as moving from one column address to the next higher one and stepping down the screen from one line to the next is simply an operation of incrementing the Row Address.

A carriage return is simply a means of telling the Column Address register to return to an address of zero. The registers are therefore nothing more than counters which react to asynchronous signals generated at the user's command.

UP/DOWN FACILITY

To add flexibility we have chosen to make the counters reversible so that, if desired, we can step the address codes in the other direction—this enables back spacing and stepping UP the screen for correction purposes.

It would have been possible to incorporate a "tab" facility so that, at a touch of a button, the column address register would take up a pre-determined code which might be of help in compiling tables of numbers. We felt that this was an un-necessary luxury and although simple in theory would have complicated the wiring of the system.

The only condition we have built in, of this nature, is "Reset to Zero" which zeros the address codes for both columns and rows. This enables the user to do a rapid return to the top left hand corner of the screen to start a page of type.

IC35 forms the Row Address Register. Like all the counters used in this part of the circuit it is an UP/DOWN counter that receives its direction instruction at pin 5. In this case the instruction is generated by a flip flop (IC32a). One press of the Forward/Reverse control key will make the counters operate in an UP mode and a second press will toggle the flip flop making them count down. A "0" on pin 11 of IC35 will reset it to zero in this circuit and this signal is obtained from SW2. Counting pulses (for stepping from one row to the next) are generated by the Line Feed key of the keyboard and this signal is detected by the keyboard interface

circuitry (to be described later) and fed to pin 14 of the Row Address Register.

DEAD END COUNTERS

There are 16 discrete row address codes and the four binary stages within IC35 are a perfect match. This allows us to use another feature of this integrated circuit. It has a Maximum/Minimum count output at pin 12. When the counter reaches "All Ones" when counting UP this output goes to "1" and the same happens when the counter reaches "All Noughts" when counting DOWN. By feeding this signal back to the enable input of the circuit it allows us to turn the unit into a "Dead End Counter". This facility ensures that when the bottom row of the screen is reached a further depression of the line feed button does not set the counter back to zero—which would result in the writing position jumping back to the top row of the screen.

Because the outputs of this stage correspond to the Row Address Waveforms as generated by the Row Address Counter we give them similar designations suffixed by an "a". They are Q33a, 34a, 35a and Q36a. They are eventually compared with their equivalents Q33, 34, 35 and Q36 in the comparator comprising ICs29 to 31 but more about this later.

The Column Address Register works on exactly the same principle. IC36 is a four stage UP/DOWN counter as is IC37 which provides the fifth bit of the comparison address. These two integrated counters are cascaded one into the next and both receive their direction instruction from the same flip flop as the Row Address Register. This register has to increment, every time a character key is depressed, on the release of the key. It also has to increment on receipt of the non-writing "Cursor Step" signal. These two signals are combined in the keyboard interface circuit and we see their combined signal (called Character Step) coming in to pin 14 of IC36.

To prevent the register cycling round to restart addresses for the row in question we again have to make it a "Dead End Counter". This is rather more complicated than for the Row Address Register because we cannot make use of the Maximum/Minimum signal from IC37 directly. This is because only its first stage is used. We therefore have the

Fig. 19. The schematic diagram of the "Up/Down" Counter, the Row Address Register, the Column Address Register, the Comparitor and the "Direction Indicators".

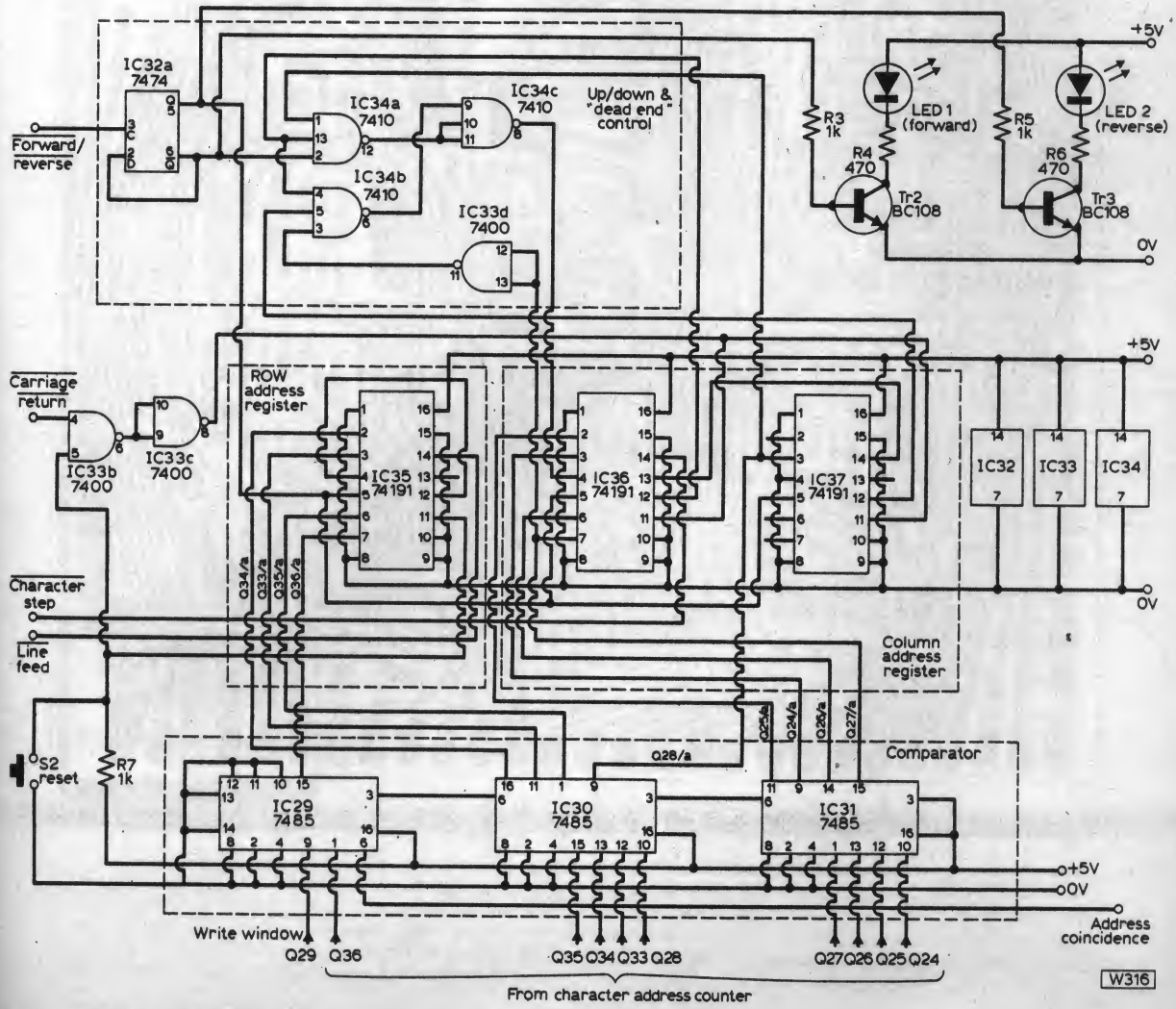


Fig. 20. The major portion of the wiring pattern on the etched board. The remaining pattern is on the component side of the board and can be seen as Fig. 21.

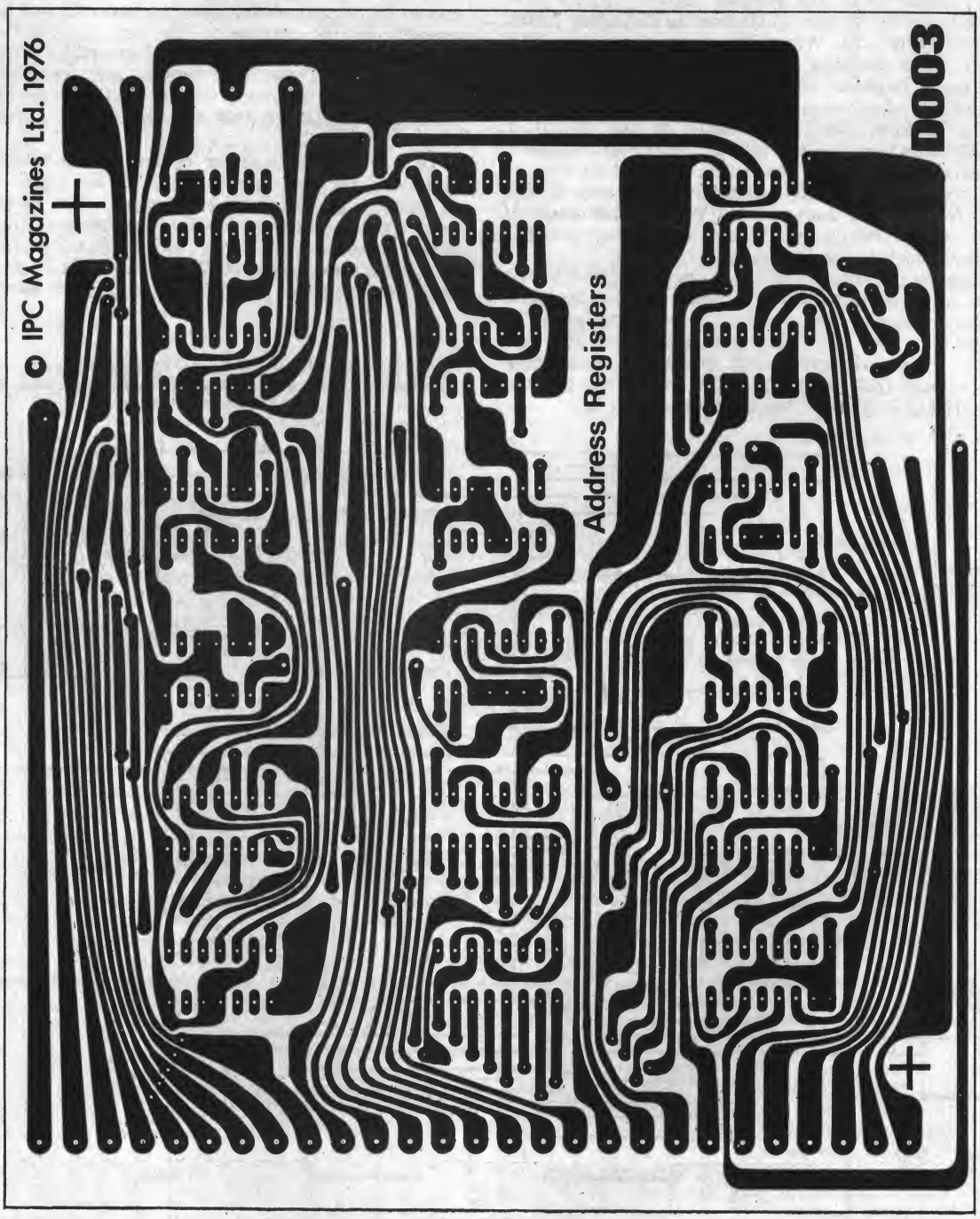
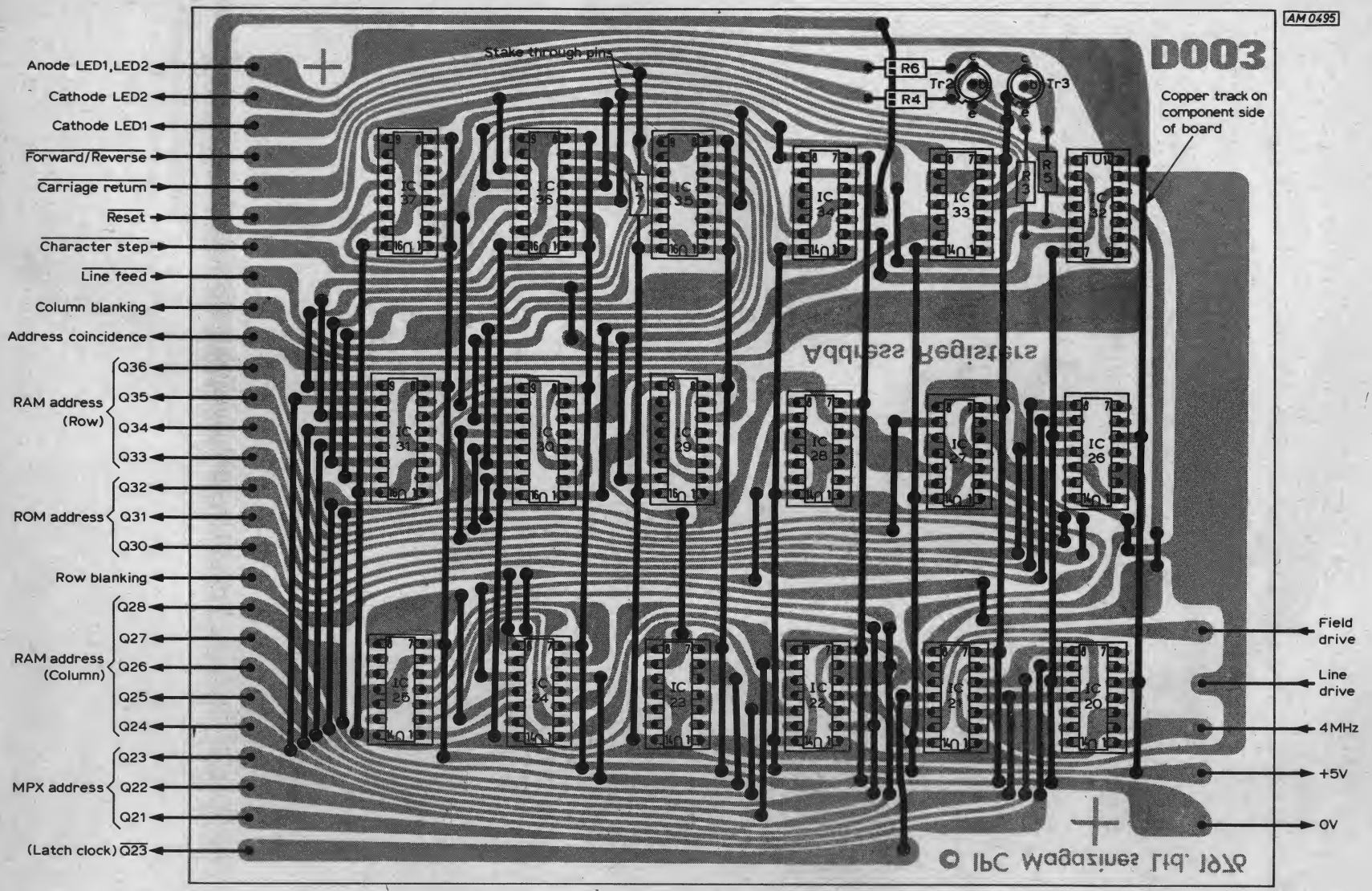


Fig. 21. The component locations on the board. Note that IC32 is reversed in orientation compared to all the other ICs on this board. Since R7 acts as a stake between the two sides of the board it is essential to solder both sides of both ends.


AM 0495
D003
Stake through pins
Copper track on component side of board
R6
R4
Tr2
Tr3
Anode LED1,LED2
Cathode LED2
Cathode LED1
Forward/Reverse
Carriage return
Reset
Character step
Line feed
Column blanking
Address coincidence
RAM address (Row)
Q36
Q35
Q34
Q33
ROM address
Q32
Q31
Q30
Row blanking
RAM address (Column)
Q28
Q27
Q26
Q25
Q24
MPX address
Q23
Q22
Q21
(Latch clock) Q23
Field drive
Line drive
4MHz
+5V
0V
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circuitry comprising IC33d and IC34a, b and c which detects the state of the counter and depending on the direction of counting and the state of the count it will activate, or de-activate, the enable input of IC36 (pin 4). Again it is convenient to be able to reset the register to "All Zeros" for an instant return to the left hand end of a row but in this instance we have to consider two sources of the reset signal. It might come from the reset button (SW2) which is used for starting from the top left hand corner of the screen or from the Carriage Return signal generated from the keyboard. These two signals are combined in IC33b and c before being fed to the reset inputs of the Column Address Register.

COMPARATOR

The five outputs, Q24a, 25a, 26a, 27a and Q28a are fed to other stages of the comparator with their counterparts from the Column Address Counter. If we consider the four Row Address bits and the five Column Address bits together we can define any one of the 512 possible positions of character cells with a nine bit word. Provided we compare like bit with like (from the counter and register respectively) there will only be a perfect comparison of all nine pairs of bits when the Address Counter is addressing the cell position defined by the Register. Our comparator therefore has to be capable of handling nine pairs of variables and when coincidence occurs it must produce an output which is later used to generate the Write instruction.

We call the comparator's output "Address Coincidence." Note that we have one extra signal coming into the comparator at pin 9 of IC29; this is the Write Window which has already been described. We can use it at this stage to inhibit the generation of an Address Coincidence signal during the left and right hand margins by simply comparing it against logic level "O". When the Write Window is at "O" and we have a perfect match of addresses the Address Coincidence signal goes "high".

DIRECTION INDICATOR

Because a toggling flip flop is used to control the direction of the registers it would not be clear which way they were likely to go without some form of indicator. LEDs 1 and 2 are driven from the Q and $\overline{Q}$ outputs of the direction change flip flop. When LED1 is lit it indicates "Forward" operation whereas LED2 indicates "Reverse" operation.

CONSTRUCTION

The inter-component wiring for this unit is again provided by a double sided PCB. The major portion is shown in Fig 20, whilst the "overflow" is combined with the component layout of Fig 21.

From Fig 21 it is clear that most of the construction consists of inserting integrated circuits into their correct holes. However, we make no apology for repeating our previous warnings, namely:— check the orientation of the devices, ensure no pins are folded under, keep the heat from the soldering iron to a minimum and solder all the stakes on both sides. On the subject of stakes, note that R7 acts as a stake so each side of each end needs to be soldered.

IMPORTANT CONSTRUCTIONAL NOTE

To prevent erratic logic conditions arising from current spiking—caused by the very high switching speeds of TTL and the heavy current drawn by its output during switching operations—it is usual to incorporate small value capacitors across the power rails. When the prototype was originally designed it was felt that these capacitors could be soldered across the power supply leads on the top of each board. As it turned out, there were no problems with spurious pulses hence the illustrations of the boards do not show the capacitors. If, after construction, there is any indication of erratic operation the constructor should connect four 0·22uF capacitors between the +5V and OV rails at convenient positions on each board. These can be soldered directly to the topside printed wiring—if double sided boards are used. They should be distributed so that the de-coupling effect of each will affect as many of the IC packages as possible. There are no rules for this but, equally, there are unlikely to be any problems if the recommended layout is adopted.

You will notice that provision is made for flying leads to be taken to the two LEDs which should be mounted on the front panel in a convenient position. On the prototype there was room for them on the keyboard metalwork.

The third major board of the three, containing the Memories, the Keyboard Interface, The Cursor Generator and the Video Stages will be covered in our December issue.

★ components list

Address Counter/Register/Comparitor

Integrated Circuits

IC20	SN7493
IC21	SN7400
IC22	SN74177
IC23	SN74177
IC24	SN7404
IC25	SN7430
IC26	SN7493
IC27	SN74177
IC28	SN74177
IC29	SN7485
IC30	SN7485
IC31	SN7485
IC32	SN7474
IC33	SN7400
IC34	SN7410
IC35	SN74191
IC36	SN74191
IC37	SN74191

Resistors

R3	1k	10%, ¼W
R4	470	10%, ¼W
R5	1k	10%, ¼W
R6	470	10%, ¼W
R7	1k	10%, ¼W

Semiconductors

Tr2 BC108
Tr3 BC108
LED1 MV5025 or similar
LED2 MV5025 or similar

Miscellaneous

Printed circuit board, code D003, from Readers PCB Service. Dil sockets, 12 off 14 way and 6 off 16 way (DIL strip sockets could be used). Tinned copper wire for staking. Board pins.